BCA Semester-II (Hons) Examination, 2022-23
BACHELOR OF COMPUTER APPLICATION

Course ID : 23311 **Course Code : CC-03**

Course Title : Digital Logic

Time : 2 Hours Full Marks : 50

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

1. Choose the best alternative from the following options for each question: 1×10=10

   i) A Boolean function $x'+y'+xy+x'y$ is equivalent to-

   a) $x'+y'$

   b) $x+y$

   c) $x+y'$

   d) $x'+y$

   e) None of the above

   ii) In an SR latch made by cross coupling two NAND gates, if both S and R inputs are set to 0 then it will result in

   a) Q=0, Q′=1

   b) Q=1, Q′=0

   c) Q=1, Q′=1

   d) Indeterminate states

   e) None of the above

   iii) The hexadecimal representation of 657_8 is:

   a) 1AF

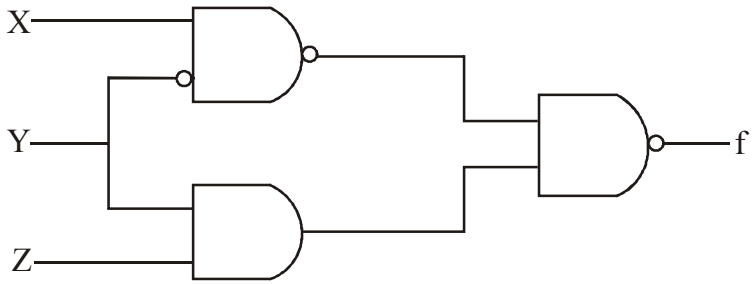
   b) D78

   c) D71

   d) 32F

   e) None of the above.

   iv) Consider the following circuit, which one of the following is TRUE?



   a) f is independent of x

   b) f is independent of y

   c) f is independent of z

   d) the value of f is 1

   e) None of the above.

v) What value is to be considered for don't care condition?

a) 0

b) 1

c) Either 0 or 1

d) Any number except 0 and 1

e) None of the above

vi) Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

a) 2^n lines to 1 line

b) 2^{n+1} lines to 1 line

c) 2^{n-1} lines to 1 line

d) 2^{n-2} lines to 1 line

e) None of the above.

vii) Race around condition is avoided in-

a) JK Flip flop

b) Master Slave Flip flop

c) SR Flip flop

d) SR latch

e) None of the above.

viii) The size of PLA is specified by number of-

a) Inputs

b) Product terms

c) Outputs

d) All of the above

e) None of the above.

ix) Consider the following function:

$F_1 = \Sigma(1,2,4,8,10,l4)$

$F_2 = \Sigma(2,5,9,1l)$

$F_3 = \Sigma(2,4,5,6,7)$

The minimum configuration of the decoder should be

a) 2×4

b) 3×8

c) 4×16

d) 5×32

e) None of the above.

x) The operation which is commutative but not associative is:

a) AND

b) OR

c) EX-OR

d) NAND

e) None of the above.

GROUP-B

2. Answer any **five** questions: 2×5=10

i) Explain Minterm and Maxterm.

ii) Differentiate positive and negative logic system.

iii) Express any one the following decimal numbers in 2421 and 5421 codes:

a) 6734

b) 3421

iv) What is non Weighted code? How it differ from weighted code?

v) What is the function of a multiplexer's select inputs?

vi) What is shift register? Name the different types of shift registers.

vii) What is meant by edge triggering?

viii) Explain the difference between the performance of asynchronous and synchronous counters.

GROUP-C

3. Answer any **four** questions: 5×4=20

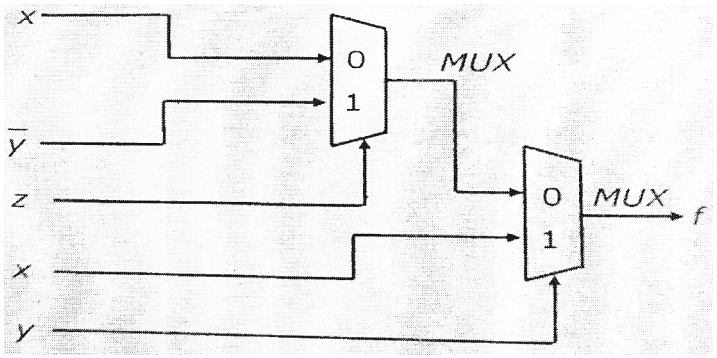
i) A circuit outputs a digit in the form of 4 bits.0 represented by 0000, 1 by 0001 ...9 by 1001. A combinational circuit is to be designed which takes these 4 bits as inputs and outputs 1 if the digit ≥ 5, and 0 otherwise. If only basic gates are used then what is the minimum number of gates required. Draw the circuit diagram and truth table.

ii) Prove that:

a) $BCD+AC'D'+ABD=BCD+AC'D'+ABC'$

b) $A'B'C'+A'B'C+A'BC'+A'BC+AB'C'=A'+(B+C)'$

iii) Consider the following circuit below. Write down the output of the circuit :



iv) Design a full adder circuit using two half adder. Write down the truth table of full adder.

v) Explain how a J-K flip flop can be converted into a D flipflop.

vi) Draw the logic diagram of three bit synchronous binary up-counter.

GROUP-D

4. Answer any **one** from the followings: 10×l=10

i) a) Simplify the Boolean function using Quine McClusky method :

$F(W, X, Y, Z)=\Sigma_m(l,3,4,5,9,l0,l1)+\Sigma_d(6,8)$

b) Implement the function using decoder:

$F(A, B, C)=\Sigma_m(1, 3, 5, 6)$ 6+4

ii) a) Write truth table, circuit diagram and excitation table of T-flip flop.

b) Write a short note on parallel-in-parallel-out shift register. 6+4

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